

ICE15N65FP N-Channel Enhancement Mode MOSFET

RoHS compliant
2011/65/EU



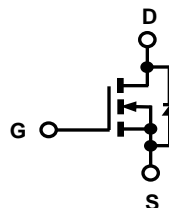
HALOGEN FREE

| Product Summary | | | |
|-----------------|------------------------|---------------|-----|
| I_D | $T_A=25^\circ\text{C}$ | 15A | Max |
| $V_{(BR)DSS}$ | $I_D=250\mu\text{A}$ | 650V | Min |
| $r_{DS(on)}$ | $V_{GS}=10\text{V}$ | 0.25 Ω | Typ |
| Q_g | $V_{DS}=480\text{V}$ | 59nC | Typ |

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dv/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 TO 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.



**T0220 Full-PAK
Isolated (T0-220)**

Maximum ratings^b, at $T_j=25^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|-----------------------------------|----------------|--|-------------|------------------|
| Continuous drain current | I_D | $T_c=25^\circ\text{C}$ | 15 | A |
| Pulsed drain current | $I_{D, pulse}$ | $T_c=25^\circ\text{C}$ | 45 | A |
| Avalanche energy, single pulse | E_{AS} | $I_D=7.5\text{A}$ | 460 | mJ |
| Avalanche current, repetitive | I_{AR} | limited by T_j max | 7.5 | A |
| MOSFET dv/dt ruggedness | dv/dt | $V_{DS}=480\text{V}$, $I_D=15\text{A}$, $T_j=125^\circ\text{C}$ | 50 | V/ns |
| Gate source voltage | V_{GS} | Static | ± 20 | V |
| | | AC ($f > 1\text{Hz}$) | ± 30 | |
| Power dissipation | P_{tot} | $T_c=25^\circ\text{C}$ | 35 | W |
| Operating and storage temperature | T_j, T_{stg} | | -55 to +150 | $^\circ\text{C}$ |
| Mounting torque | | M 2.5 screws | 50 | Ncm |

a When mounted on 1inch square 2oz copper clad FR-4

b Preliminary Data Sheet – Specifications subject to change

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|-----|-----|------|
| | | | Min | Typ | Max | |

Thermal characteristics

| | | | | | | |
|---|------------|-------------------------------------|---|---|-----|------|
| Thermal resistance, junction-case ^a | R_{thJC} | | - | - | 3.5 | °C/W |
| Thermal resistance, junction-ambient ^a | R_{thJA} | leaded | - | - | 80 | |
| Soldering temperature, wave soldering only allowed at leads | T_{sold} | 1.6mm (0.063in.) from case for 10 s | - | - | 260 | °C |

Electrical characteristics ^b, at $T_j=25^{\circ}\text{C}$, unless otherwise specified

Static characteristics

| | | | | | | |
|----------------------------------|---------------|---|-----|------|------|---------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0\text{ V}, I_D=250\mu\text{A}$ | 650 | 675 | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=250\mu\text{A}$ | 2.1 | - | 3.9 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_j=25^{\circ}\text{C}$ | - | 0.1 | 1 | μA |
| | | $V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_j=150^{\circ}\text{C}$ | - | - | 100 | |
| Gate source leakage current | I_{GSS} | $V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$ | - | - | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=10\text{V}, I_D=7.5\text{A}, T_j=25^{\circ}\text{C}$ | - | 0.25 | 0.28 | Ω |
| | | $V_{GS}=10\text{V}, I_D=7.5\text{A}, T_j=150^{\circ}\text{C}$ | - | 0.62 | - | |
| Gate resistance | R_G | $f=1\text{ MHz}, \text{open drain}$ | - | 4.7 | - | Ω |

Dynamic characteristics

| | | | | | | |
|------------------------------|--------------|---|---|------|---|---------------|
| Input capacitance | C_{iss} | $V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$ | - | 1800 | - | μF |
| Output capacitance | C_{oss} | | - | 600 | - | |
| Reverse transfer capacitance | C_{rss} | | - | 5 | - | |
| Transconductance | g_{fs} | $V_{DS}>2 \cdot I_D \cdot R_{DS}, I_D=7.5\text{A}$ | - | 15 | - | S |
| Turn-on delay time | $t_{d(on)}$ | $V_{DS}=380\text{V}, V_{GS}=10\text{V}, I_D=15\text{A}, R_G=4\Omega \text{ (External)}$ | - | 39 | - | ns |
| Rise time | t_r | | - | 10 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 55 | - | |
| Fall time | t_f | | - | 6 | - | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|-----|-----|------|
| | | | Min | Typ | Max | |

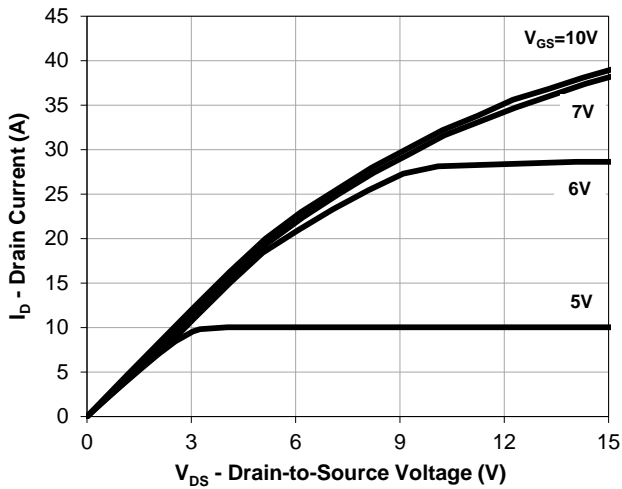
Gate charge characteristics

| | | | | | | |
|-----------------------|----------------------|---|---|-----|---|----|
| Gate to source charge | Q_{gs} | $V_{DS}=480\text{ V}, I_D=15\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$ | - | 11 | - | nC |
| Gate to drain charge | Q_{gd} | | - | 18 | - | |
| Gate charge total | Q_g | | - | 59 | - | |
| Gate plateau voltage | V_{plateau} | | - | 5.5 | - | V |

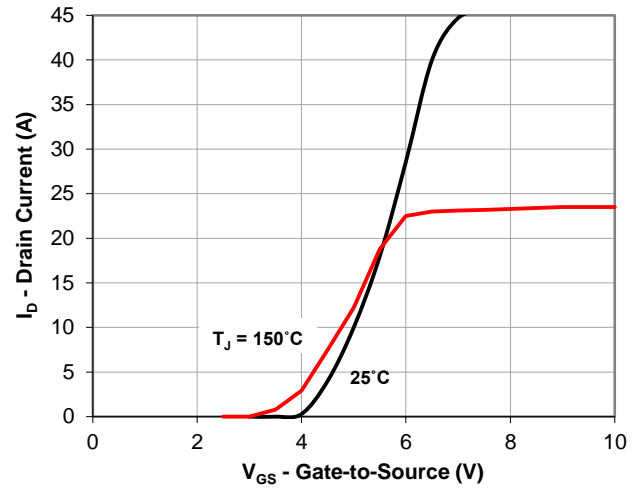
Reverse Diode

| | | | | | | |
|-------------------------------|----------|--|---|-----|-----|---------------|
| Diode forward voltage | V_{SD} | $V_{GS}=0\text{ V}, I_S=I_F$ | - | 0.9 | 1.2 | V |
| Reverse recovery time | t_{rr} | $V_{RR}=480\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{S}$ | - | 400 | - | ns |
| Reverse recovery charge | Q_{rr} | | - | 6 | - | μC |
| Peak reverse recovery current | I_{rm} | | - | 35 | - | A |

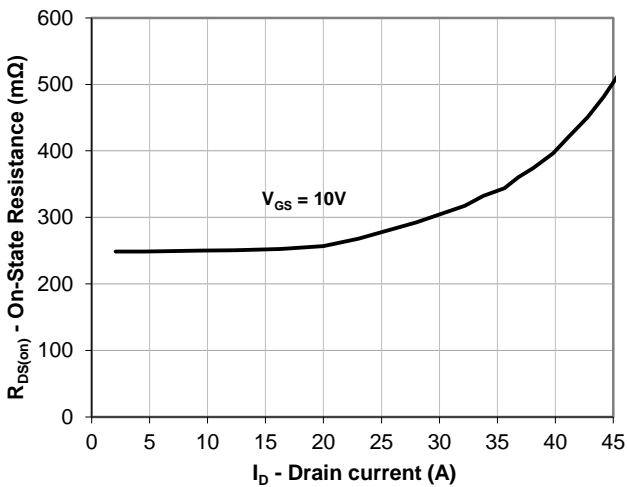
Output Characteristics



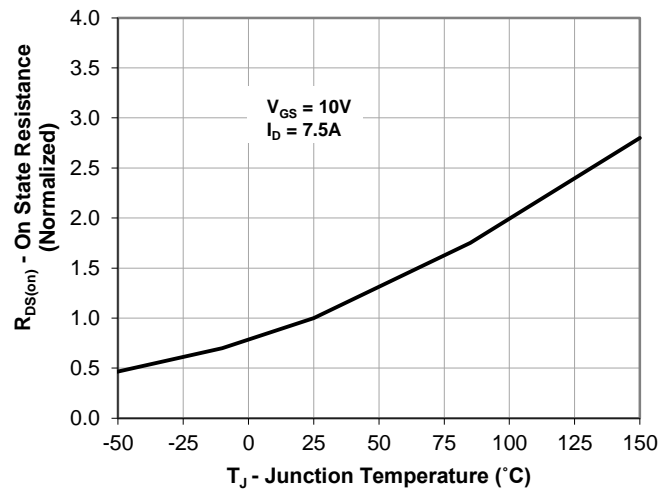
Transfer Characteristics



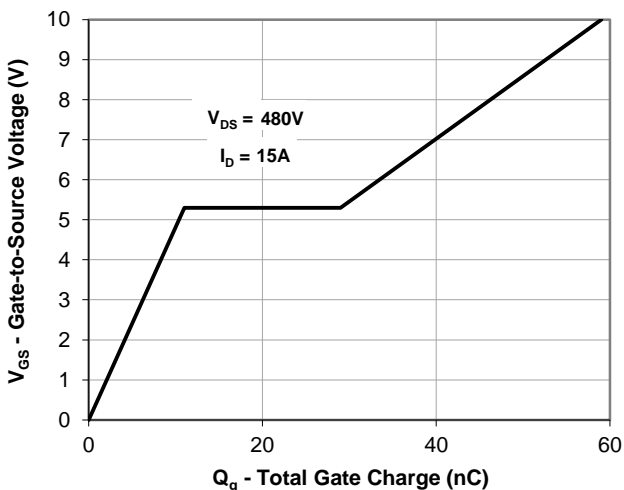
On Resistance vs Drain Current



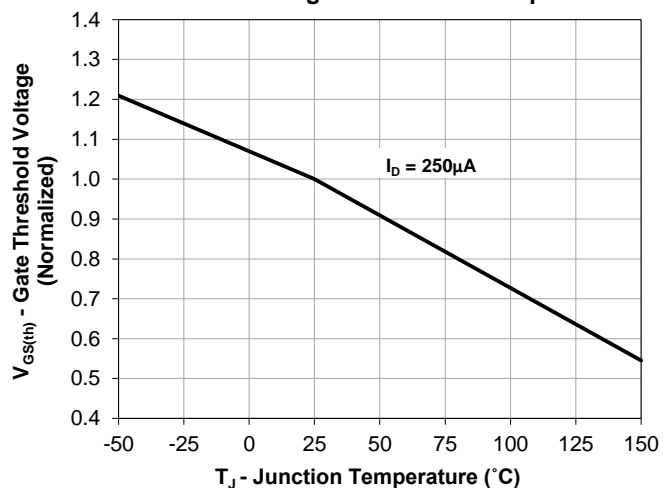
On Resistance vs Junction Temperature



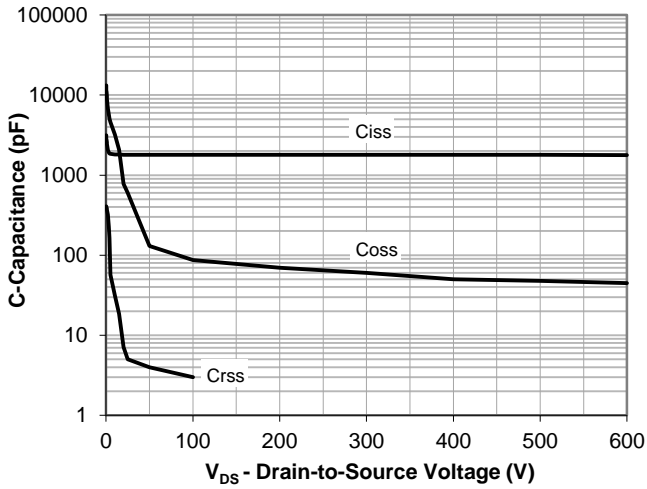
Gate Charge



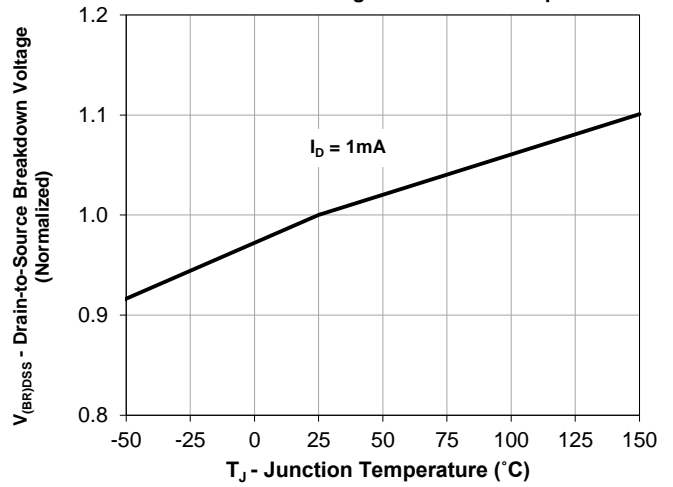
Gate Threshold Voltage vs Junction Temperature



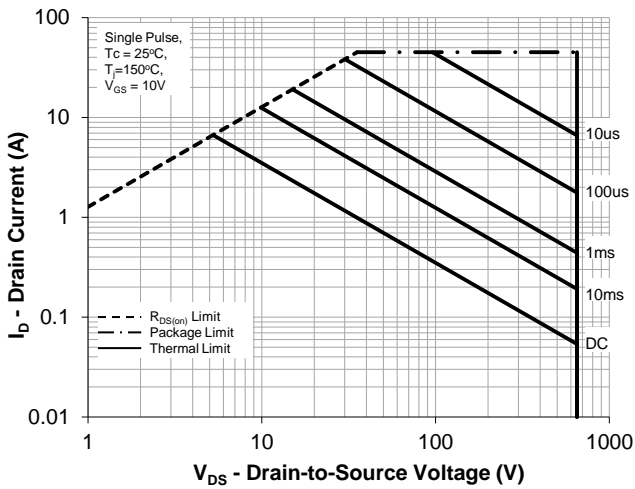
Capacitance



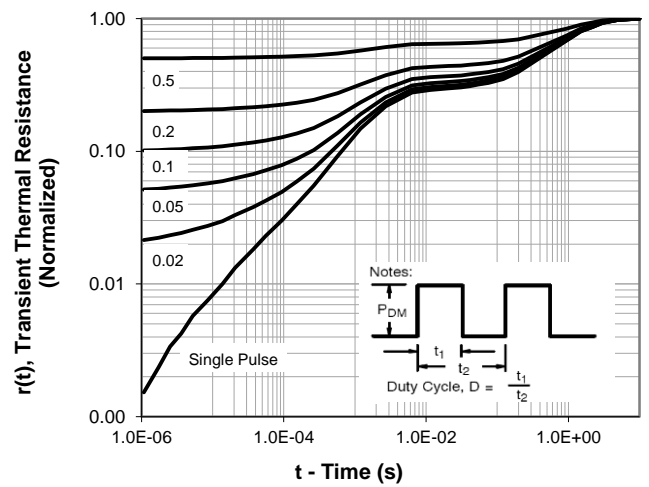
Drain-to-Source Breakdown Voltage vs. Junction Temperature

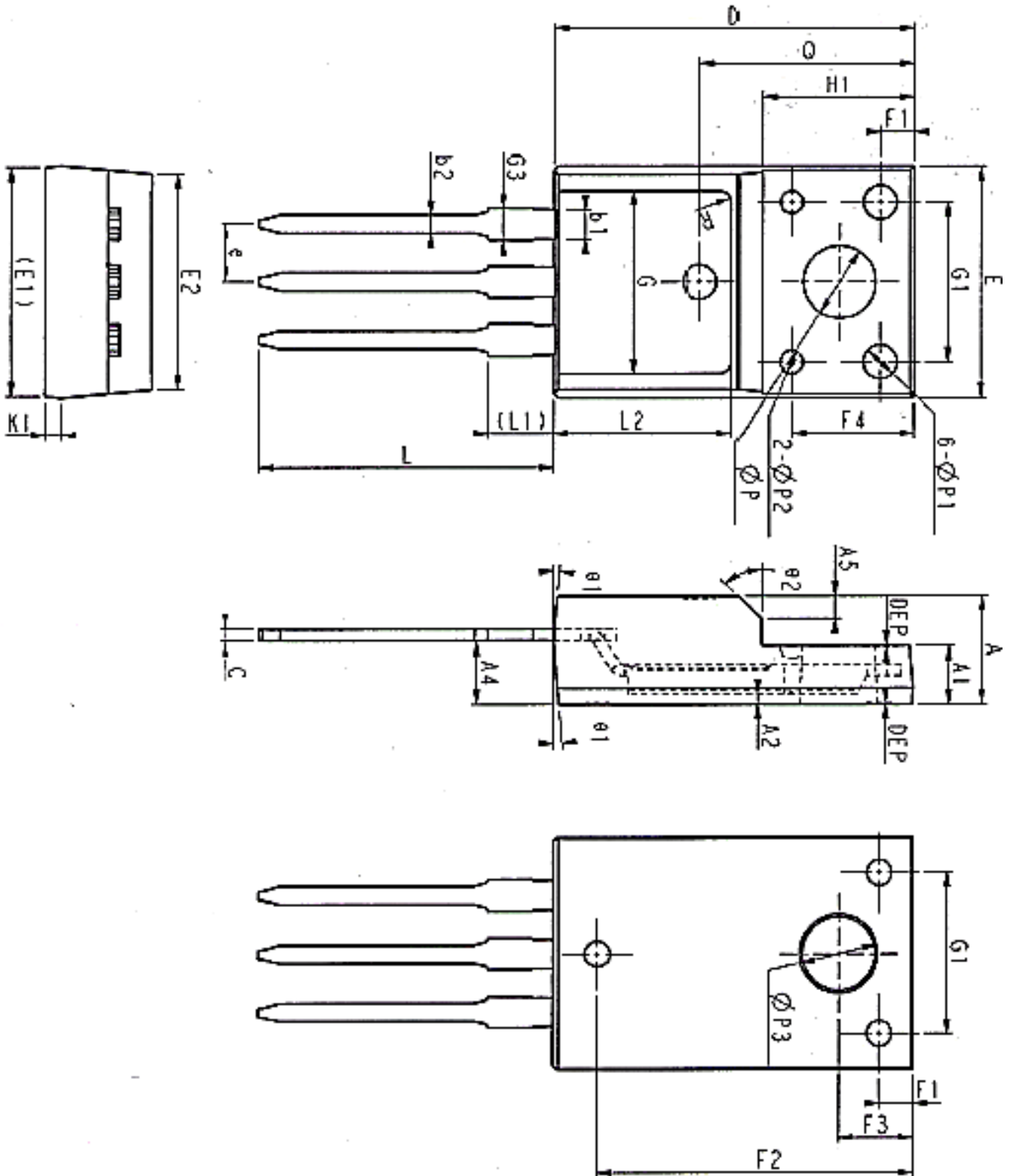


Maximum Rated Forward Biased Safe Operating Area



Transient Thermal Response, Junction-to-Case





| COMMON DIMENSIONS | | | | | | |
|-------------------|---------|-------|-------|----------|-------|-------|
| SYMBOL | MM | | | INCH | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| E | 9.63 | 10.19 | 10.75 | 0.38 | 0.40 | 0.42 |
| E1 | 9.94 | 10.04 | 10.14 | 0.39 | 0.40 | 0.40 |
| E2 | 9.36 | 9.46 | 9.56 | 0.37 | 0.37 | 0.38 |
| A | 4.30 | 4.60 | 4.90 | 0.17 | 0.18 | 0.19 |
| A1 | 2.34 | 2.77 | 3.20 | 0.092 | 0.11 | 0.126 |
| A2 | 0.43 | 0.87 | 1.30 | 0.017 | 0.03 | 0.051 |
| A4 | 2.51 | 2.72 | 2.93 | 0.10 | 0.11 | 0.12 |
| A5 | 1.00REF | | | 0.39REF | | |
| c | 0.33 | 0.54 | 0.75 | 0.013 | 0.021 | 0.030 |
| D | 15.67 | 15.9 | 16.13 | 0.617 | 0.626 | 0.635 |
| Q | 9.4REF | | | 0.370REF | | |
| H1 | 6.7REF | | | 0.264REF | | |
| E | 2.54BSC | | | 0.100BSC | | |
| ΦP | 3.18REF | | | 0.125REF | | |
| L | 12.78 | 13.25 | 13.72 | 0.50 | 0.52 | 0.54 |
| L1 | 2.83 | 3.25 | 3.67 | 0.11 | 0.13 | 0.14 |
| L2 | 7.70 | 7.80 | 7.90 | 0.30 | 0.31 | 0.31 |
| ΦP1 | 1.4 | 1.5 | 1.6 | 0.055 | 0.059 | 0.063 |
| ΦP2 | 1.15 | 1.2 | 1.25 | 0.045 | 0.047 | 0.049 |
| ΦP3 | 3.45REF | | | 0.136REF | | |
| θ1 | 3° | 5° | 7° | 3° | 5° | 7° |
| θ2 | - | 45° | - | - | 45° | - |
| DEP | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| F1 | 1.0 | 1.50 | 2.0 | 0.039 | 0.059 | 0.079 |
| F2 | 13.8 | 13.90 | 14.0 | 0.543 | 0.547 | 0.551 |
| F3 | 3.20 | 3.30 | 3.40 | 0.126 | 0.130 | 0.134 |
| F4 | 5.30 | 5.40 | 5.50 | 0.209 | 0.213 | 0.217 |
| G | 7.80 | 8.00 | 8.20 | 0.307 | 0.315 | 0.323 |
| G1 | 6.05 | 6.58 | 7.10 | 0.238 | 0.259 | 0.280 |
| G3 | 1.25 | 1.35 | 1.45 | 0.049 | 0.053 | 0.057 |
| b1 | 1.23 | 1.31 | 1.38 | 0.048 | 0.051 | 0.054 |
| b2 | 0.61 | 0.78 | 0.94 | 0.024 | 0.031 | 0.037 |
| K1 | 0.65 | 0.70 | 0.75 | 0.026 | 0.028 | 0.030 |
| R | 0.50REF | | | 0.020REF | | |

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2
US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.

Marking Information

YY = Last two digits of the year

WW = Work week calendar on Icemos subcon assembly & test house

***** = Initial for Icemos subcon assembly and test house

XXXX = Wafer Lot ID

00 = may be used for wafer ID in a special case.

= "00" is used unless specified.

ICE15N65 = ICE is Icemos logo and 15N65 is a designated device part number

